A Universal Controller for Parallel Inverters with Fuzzy Logic Controller

Under Various Operating conditions

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Abstract—this article proposes a universal controller for operating parallel inverters in both grid-connected (GC) and freestanding (SA) modes and ensuring seamless transition between them without changing the control structure. The suggested fuzzy logic controller accurately adjusts the grid current of a single inverter in the GC mode. The suggested fuzzy logic controller may automatically switch from grid current control to v C-i g-based droop control when islanding occurs; no crucial islanding detection is required. There are various advantages to using this universal controller. First, it can realize seamless transfer of parallel inverters; Micro grid reliability can be guaranteed in the SA state, and power sharing can be achieved among parallel inverters without communication lines. Second, compared with droop control, it can regulate the grid current accurately and output constant power when the grid voltage fluctuates in the GC state. Third, the grid current harmonics in the GC state and capacitor voltage harmonics in the SA state can be mitigated. Simulation and experimental results verify the effectiveness of the controller.

Index Terms—Current droop control, grid-connected (GC) state, seamless transfer, standalone (SA) state.

I.INTRODUCTION

Appropriated energy assets (DERs) have drawn in expanding insightful consideration since they can lighten pressure in primary transmission frameworks, further develop framework power quality, and lessen ecological contamination. The far reaching infiltration of DERs interfaced through power converters has presented the idea of miniature networks (MGs). A MG is a limited scale framework comprising of various DERs; electrical energy stockpiling gadgets; and burdens that are electrically interconnected and progressively controlled, which can work in both matrix associated (GC) and independent (SA) states. The yield voltage and yield force of DERs are constrained by controlling inverters to accomplish the accompanying objectives under various MG working states as indicated by framework accessibility.

1) Controlling the yield force of inverters in the GC state as indicated by set focuses dictated by the MG focal regulator (MGCC).

2) Maintaining the steadiness of MG and burden voltage by means of burden following (i.e., keeping a harmony among creation and utilization) while progressing from the GC state to SA state.

3) Voltage guideline and exact force partaking in the SA states [1].Compared with targets (1) and (3) in a consistent express, an essential test includes consistent exchange from the GC state to SA state. The control focuses in GC and SA states are discernibly unique, which might trouble highway moves with inrush

flows and potential framework crashes [2]. Along these lines, two significant control systems have been proposed to acknowledge consistent exchange from the GC state to SA state. The principal approach is the half breed current and voltage mode (HCVM) control strategy, and the second is the hang control technique. In the HCVM control technique, the DER inverter works under a current control mode (CCM) in the GC state however a voltage control mode (VCM) in the SA state [3]–[11]. In the GC express, these inverters can work in corresponding with different inverters dependent on dynamic and responsive force (PQ) control. Most inverters having a place with DER frameworks work in CCMs, as in photovoltaic (PV) or wind power frameworks. These inverters can take part in the control of the MG ac voltage sufficiency and recurrence by changing, at a more elevated level control layer, the references of dynamic and responsive forces to be conveyed [1]; notwithstanding, inverters with CCM can't work in the SA state in case there is no inverter to set the MG voltage abundancy and recurrence. Somewhere around one inverter ought to along these lines change to VCM in the SA state, and it is important to switch between two regulator sets relying upon the state. This errand requires a basic islanding identification conspire, which expands framework intricacy; the islanding discovery requires time, shifting from 20 ms to a couple hundred ms. From the second a utility blackout starts (i.e., islanding happens) to the second the regulator is changed to VCM (i.e., islanding is distinguished), the heap voltage is neither fixed by the utility nor directed by the inverter. Accordingly, the load voltage quality may worsen during this period [12]. Various improved HCVM control methods have been proposed to overcome this drawback by switching the inverter from a CCM to a VCM without relying on islanding detection. When the grid is broken, some limiters in the control structure of the inverter will become saturated [13]–[19] or desaturated [12] to realize automatic switching of the control mode; therefore, the load voltage quality can be improved during the transition from the GC state to SA state. However, many of these improved HCVM control methods mainly focus on the seamless transfer of a single inverter. If an improved HCVM control method is applied to parallel inverters, they cannot operate normally in the SA state. They will change to constant amplitude and constant frequency (V-f) controlled voltage sources in the SA state, which will elicit a circulating current and prevent power sharing among them. Under the droop control method, including virtual synchronous generator control as a special case, the parallel inverters in DERs operate in VCMs in GC and SA states. The droop control method is suitable for inverters in energy storage (ES) systems or for PV or wind power systems with ES equipment. These inverters can help regulate MG frequency and voltage by delivering appropriate active and reactive power values in GC and SA states. They can achieve seamless transfer from the GC state to SA state and realize power sharing in the SA state. However, if grid voltage fluctuates in the GC state, the objective (1) may fail and the inverter output power could deviate from its set point. Moreover, the droop control method does not control the inverter grid current directly; hence, its dynamics may be slow and distortion could follow from grid voltage harmonics. Several improved droop control methods have been devised to solve these issues [2], [20]–[28]. An enhanced power flow control for droop-controlled inverters was suggested in [20], where the feed forward of grid frequency and voltage magnitude was adopted to mitigate the effects of grid fluctuation; however, reference switching occurred in different operating states. Control strategies for multimode operations of an online uninterruptible power supply (UPS) system were proposed [21], where UPS system inverters were based on droop control. The transfer between different operating modes was achieved by adjusting the reference value and control structure of droop control. Yet, the reference switching in [20] and adjustment to the reference and control structure in [21] both relied on islanding detection. If islanding occurs but has not yet been detected and the reference and control structure remain constant, undesirable transients may result. Karimi-Ghartemani et al. [22] presented a controller that was flexible in combining real and reactive power control with voltage and frequency support, which did not rely on islanding detection, but the grid current was still not controlled directly. This article tries to

address the above-mentioned research gaps by proposing a universal controller for parallel inverters. The universal controller is mainly composed of frequencylocked-loop (FLL) and three cascaded control loops: a grid current loop, capacitor voltage loop, and inductor current loop. A proportional-integral (PI) regulator is adopted in the grid current loop, and a limiter is inserted after the integrator. A PI regulator is adopted in the capacitor voltage loop, and a proportional (P)-regulator is adopted in the inductor current loop. The proposed universal controller offers three advantages. 1) In the GC state, parallel inverters are controlled as current sources, and the grid current of an individual inverter is regulated by a PI regulator in the grid current loop to follow its reference value. Compared with the droop control method, the universal controller can regulate the grid current accurately and output constant power when the grid voltage fluctuates in the GC state. 2) When islanding occurs, the integrator in the grid current loop will be saturated, but the P-regulator will continue working and the inverters will transfer automatically from current sources to voltage sources based on 〖_〗 vC–ig droop control without relying on islanding detection. The droop relationship is established between the inverter output capacitor voltage VC and grid current ig in the dq synchronous reference frame (SRF). Seamless transfer of parallel inverters is achieved, and uninterruptible load voltage is realized during the state transition. In the SA state, the combination of vC–ig droop control and an FLL block can realize power sharing among parallel inverters without communication lines. 3) Additionally, quasi-resonant (QR) controllers are adopted in the grid current loop and capacitor voltage loop. Compared with the droop control method, in the GC state, harmonics in the grid current caused by grid voltage distortion can be mitigated, and grid current quality can be improved. In the SA state, capacitor voltage harmonics caused by nonlinear loads connected at the point of common coupling (PCC) can be suppressed. The rest of this article is organized as follows. In Section II, the control principle of the universal controller is introduced. Section III presents the design and analysis of the control parameters. Simulation and experimental results are summarized in Sections IV and V, respectively, to verify the effectiveness of the proposed controller. Finally, conclusions are given in Section VI.

II. CONTROL PRINCIPLE OF THE UNIVERSAL CONTROLLER

In this section, the control principle of inverters with a universal controller is introduced in detail. A. System Structure a schematic diagram of parallel inverters and the main control block appear in Fig. 1. The dc voltage of the individual inverter is controlled by the front-end power electronic converter, both represented by the dc voltage source. The inverter output connects with an LC filter. Zline denotes the line impedance between the DER and PCC. The transfer switch Si is controlled by the MGCC, and the circuit breaker Su is governed by the relay protection device. When the grid is normal, Si and Su are each closed. When the grid is broken, Su turns OFF immediately, and

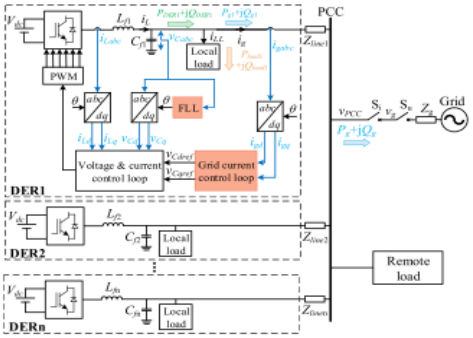
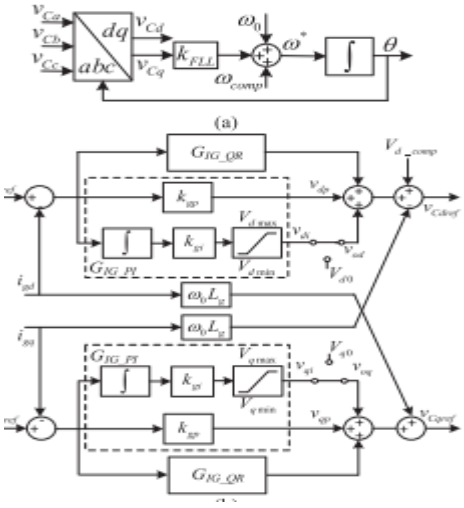


Fig. 1. Schematic diagram and control block of the universal controller



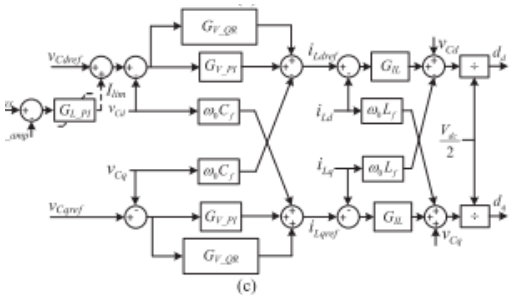


Fig. 2. Overall control diagram of the proposed controller. (a) FLL block. (b) Grid current loop. (c) Capacitor voltage loop and inductor current loop

An island forms. Once islanding is confirmed, Si turns OFF. When the grid is restored, the circuit breaker Su closes automatically. The PCC voltage should resynchronize with the utility voltage first, after which the transfer switch Si turns ON to reconnect the MG with the utility. The inductor current iLabc, capacitor voltage vCabc, and grid current igabc are sensed and used in the control loops. The PCC voltage vPCC and grid voltage vg of both sides of Si are sensed to realize resynchronization. The average model of power stage in SRF can be derived according to [15]. With the decoupling approach, the average model can be simplified into three single input single output systems, as shown in (1)–(3) and the subscript d and q are neglected

$$\frac{V_{dc}}{2}.d = L_f.\frac{d_{iL}}{dt} + R_{ESR}.i_L + v_C \quad (1)$$

$$i_L = C_f.\ \frac{dVC}{dt} + i_{LL} + i_g \quad (2)$$

$$v_C = L_{line}.\frac{d_{ig}}{dt} + R_{line}.i_{g+}v_{pcc} \quad (3)$$

where Vdc is the dc voltage, d is the average duty cycle, and RESR is the equivalent series resistance of the filter inductor Lf; iL and vC represent the inductor current and capacitor voltage, respectively; Cf is the capacitance of filter capacitor; iLL is the local load current; ig represents the grid current; Lline is the inductance component of Zline, Rline is the resistance component of Zline, and vPCC is the PCC voltage. The transfer function from capacitor voltage VC to grid current ig can be represented as (4), and the grid current can be controlled by regulating the capacitor voltage in d- and q-axes, respectively.

$$G_{igmv}(s) = \frac{i_{g(s)}}{v_{C(s)}} = \frac{1}{s.L_{line} + R_{line}} \quad (4)$$

Control Scheme The overall control block of the individual inverter is shown in Fig. 2, including the FLL block, grid current loop, capacitor voltage loop, and inductor current loop. 1) FLL Block: The FLL block is presented in Fig. 2(a); it is used instead of the phase-locked-loop (PLL) to estimate the frequency. On one hand, the FLL combines with the vCq–igq droop equation to form negative feedback control in the SA state; on the other hand, because the frequency is more stable than the phase angle, FLL is more robust against grid disturbance than PLL [29]. The compensation term ωcomp is used to realize phase angle resynchronization of the PCC voltage v_{PCC} and grid voltage vg, which will be introduced later. If the grid voltage is heavily polluted by the harmonics, the second-order generalized integrator—quadrature signal generators (SOGI-QSGs) can be used to extract the fundamental positive sequence components of capacitor voltage [30], as shown in the Appendix, which can improve the FLL performance. 2) Grid Current Loop: As indicated in Fig. 2(b), in the grid current loop, igdref and igqref denote grid current references, igd and igq are the actual grid currents on the d- and q-axes respectively; and ω0Lg is the decoupling item. A PI regulator GIG_P I and QR regulator GIG_QR are also used, where kgp represents the coefficient of the P-regulator, and kgi represents the coefficient of the integrator. One noteworthy improvement is that a limiter is inserted after the integrator rather than after the PI regulator. In the GC state, the limiter does not restrict the output of the integrator, and vod connects with vdi while voq connects with vqi; therefore, the regulator GIG_P I serves as a PI regulator to regulate the grid current to track its reference, and the inverters operate in CCMs. When the grid is broken, the limiter after the integrator becomes saturated and outputs the limiting value. The regulator GIG_P I changes to a P-regulator to form VC –ig droop control, which will be explained in detail later. The most common harmonics in grid voltage are the –5th and 7th harmonics [31], these change in the three-phase coordinating system to the –6th and 6th harmonics, respectively, in the SRF with rotating speed of fundamental angular frequency. The ±6th harmonics in the grid current are regulated to zero by the QR regulator with a resonance angular frequency of 6ω in the GC state. If harmonics of other

times occur in the grid voltage, more QR regulators with different resonance angular frequencies can be added to the grid current loop. The QR regulator has been presented in many studies [32]–[34] and is not detailed here. The compensation term Vd_comp on the d-axis is used to realize voltage amplitude resynchronization of the PCC voltage vPCC and grid voltage vg, which will be addressed later. 3) Capacitor Voltage Loop and Inductor Current Loop: Detailed structures of capacitor voltage loop and inductor current loop are depicted in Fig. 2(c), where vCd and vCq are actual capacitor voltages on the d- and q-axes, respectively; and ω0Cf is the decoupling item. Here, the voltage regulator also adopts a PI regulator GV _PI and QR regulator GV _QR. The current limitation term Ilim is added to the capacitor voltage reference to limit the inverter output current when the overload happens, where Imax is the maximum allowed output current of inverter and IL_amp is the amplitude of output current of inverter. GL_PI is a PI controller, and its upper limiting value is set as zero. iLd and iLq are the actual inductor currents on the d- and qaxes, respectively; ω0Lf is the decoupling item; and the current regulator GIL adopts a P-regulator. The capacitor voltage vCd, q is added to the d- and q-axes to implement voltage feed forward control. C. Operating Principle the operating principle of an individual inverter with a universal controller will be introduced in four states: the GC state, the transition from the GC state to SA state, the SA state, and the transition from the SA state to GC state. 1) GC State: If the utility is ideal, the grid voltage is purely sinusoidal and only includes the fundamental component. If the utility is not ideal, the grid voltage may include the fundamental component and harmonics, which will lead to harmonics in the grid current. The fundamental component in the three-phase coordinating system changes to a dc component in the SRF with a rotating speed of fundamental angular frequency. When the utility is normal, the regulator GIG_P I operates as a PI regulator to regulate the dc components if_gd and if_gq of the grid current to follow their references igdref and igqref, respectively, as shown in (5). The QR regulator GIG_QR regulates the ±6th harmonics in grid current ih6_gd,q to zero, as shown in (6)

$$\begin{cases} v_{f\_C_{dref}} = \left(k_{gp} + \frac{k_{gi}}{s}\right).\ (i_{grdef} - i_{f\_gd}) \\ v_{f_{C_{qref}}} = \left(k_{gp} + \frac{k_{gp}}{s}\right).(i_{gqref} - i_{f\_gd}) \end{cases} \quad (5)$$

$$\begin{cases} v_{f\_C_{dref}} = \frac{2_{kir6\omega cs}}{s2+2\omega_c s+(6\omega)2}.(0 - i_{h6_{gd}}) \\ v_{fC_{qref}} = \frac{2_{kir6\omega cs}}{s2+2\omega_c s+(6w)2}.(0 - i_{h6_{gq}}) \end{cases} \quad (6)$$

Where kir6 is the integral coefficient, ωc is the cut-off angular frequency, and 6ω is the resonance angular frequency of the QR regulator. The voltage reference for the capacitor voltage loop is as follows:

$$\begin{cases} v_{cdref} = v_{f\_Cdref} + v_{h\_Cdref} \\ v_{Cqref} = v_{f\_Cqref} + v_{h\_Cqref} \end{cases} (7)$$

For the capacitor voltage loop, the PI regulator GV _PI regulates the dc component of capacitor voltagevf_Cd,q to follow their references vf_Cd,qref, and the QR regulator GV _QR is used to regulate the ±6th harmonics in capacitor voltage vh_Cd,q to follow their reference vh_Cd,qref. For the inductor current loop, the P-regulator GIL is adopted to regulate the dc component and harmonics. To simplify analysis, the grid voltage is assumed as purely sinusoidal. The exchanging power between the DER and PCC can be expressed as follows

$$P_{dg} = \frac{3}{2}.(v_{Cq}\ .i_{gd} - v_{Cd}.i_{gq}) \quad (8)$$

$$Q_{dg} = \frac{3}{2}.(v_{Cq}.i_{gd-}v_{Cd}.i_{gq}) \quad (9)$$

As shown in Fig. 2(a), the phase angle of capacitor voltage is as follows

$$\theta = \frac{1}{s}.(v_{Cq}.i_{gd-v_{Cd}.v_{Cd}}.i_{gq}) \quad (10)$$

The power angle δ, namely the phase-angle difference between the capacitor voltage and PCC voltage is (11). If the grid is ideal, then the angular frequency of PCC voltage ωPCC equals the nominal angular frequency ω0

$$\delta = \frac{1}{S}\ .(\omega^* - \omega_{PCC})$$

$$=\frac{1}{S}\ .(\omega_0 + K_{FLL}\ .v_{Cq}\ - \omega_{PCC}) = \frac{1}{s}\ .(k_{FLL}.v_{Cq}) \quad (11)$$

Because of the function of the PI regulator GIG_P I in the grid current loop, the actual grid current igd and igq follow their respective references igdref and igqref. According to (5), the voltage references vCdref and vCqref also remain constant. The actual capacitor voltages vCd and vCq are regulated to follow vCdref and vCqref and remain unchanged. According

to (8) and (9), the exchanging power between the DER and PCC is kept constant. Therefore, vCq must be zero; otherwise, δ will continue

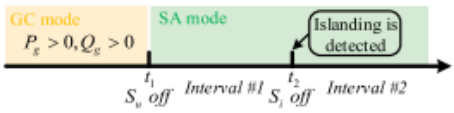


Fig. 3. Detailed transition process from the GC state to SA state

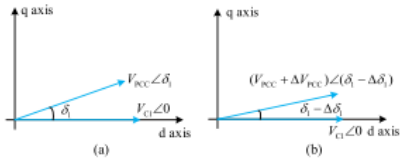


Fig. 4. (a) Phasor relationship before the utility outage. (b) Phasor relationship after the utility outage

Changing according to (11), and $_{Pdg}$ and $_{Qdg}$ will keep changing as well. Then, (8) and (9) can be simplified as follows:

$$P_{dg} = \frac{3}{2}.v_{Cd}.i_{gd} \quad (12)$$

$$Q_{dg} = \frac{3}{2}.v_{cd}.i_{gd} \quad (13)$$

2) Transition from GC State to SA State:

It is assumed that the MG injects real and reactive power into the utility in the GC state; that is, Pg. > 0 and > 0, as shown in Fig. 1. The detailed transition process from the GC state to SA state is illustrated in Fig. 3. When the grid is broken and Su turns OFF at t1, Pg and Qg each decline to zero. At this point, the output power of DERs remains nearly unchanged, and the remote load power is imposed on the output power of all DERs. Therefore, the amplitude and frequency of the remote load voltage rises and falls, respectively. Before time t1, the phasor relationship of the capacitor voltage of DER1 and the PCC voltage are shown in Fig. 4(a). The phase angle of the capacitor voltage is assumed to be 0°; thus, the phase angle of the PCC voltage is δ1. The gridcurrent of DER1 igd1 + jigq1 can be calculated as (14), where Xline1 is the reactance of Zline1, and Rline1 is the resistance of Zline1

$$i_{gd1} + ji_{gq1} = \frac{V_{C1}\angle 0 - V_{PCC}\angle\delta_1}{R_{line1}+jX_{line1}}$$

$$= \frac{V_{C1} - V_{PCC}\cos\delta 1 - jV_{PCC}\sin\delta 1}{R_{line1}+jX_{line1}} \quad (14)$$

$$i_{gd1} = \frac{(V_{C1} - V_{PCC}\cos\delta 1)R_{line1} + V_{PCC}X_{line1}\delta 1}{R_{line1}^2 + X_{line1}^2}) \quad (15)$$

$$i_{gq1} = \frac{-R_{line1}V_{PCC}\sin\delta 1 - X_{line1}(V_{C1} - V_{PCC}\cos\delta 1)}{R_{line1}^2 + R_{line1}^2} \quad (16)$$

$$i_{gd1} + ji_{gd1} = \frac{V_{C!}\angle 0 - (V_{PCC} + \Delta V_{PCC})\angle(\delta_1 - \Delta\delta_1)}{R_{line1} + jX_{line1}}$$

$$= \frac{V_{C1}}{R_{line1}+iX_{line1}} - \frac{(V_{PCC}+\Delta V_{PCC})\cos(\delta_1 - \Delta\delta_1) - j(V_{PCC}+\Delta V_{PCC})\sin(\delta_1 - \Delta\delta_1)}{R_{line1}+JX_{line1}}$$

(17)

$$i_{gd1} = \frac{(V_{PCC} + \Delta V_{PCC})X_{line1}\sin(\delta_1 - \Delta\delta_1)}{R_{line1}^2 + X_{line1}^2}$$

$$+ \frac{[V_{C1} - (V_{PCC}+\Delta V_{PCC})\cos(\delta_1 - \Delta\delta_1)]R_{line1}}{R_{line1}^2 + X_{line1}^2}$$

(18)

$$i_{gq1} = -\frac{X_{line1}[V_{C!} - (V_{PCC}+\Delta V_{PCC})\cos(\delta_1 - \Delta\delta_1)]}{R_{line1}^2 + X_{line1}^2} \frac{R_{line1}(V_{PCC}+\Delta V_{PCC})\sin(\delta_1 - \Delta\delta_1)}{R_{line1}^2 + X_{line1}^2}$$

(19)

In the MG application with low voltage, the R/X ratio of line impedance is close to 7.7 [1]. Therefore, comparing (15) and (18), the d-axis grid currentigd1 declines when the grid is broken at t1. Similarly, the q-axis grid current igq1 increases at t1 by comparing (16) and (19). As shown in Fig. 2(b), the input of the d-axis integrator in the grid current loop is larger than zero, and the output of the integrator increases. The input of the q-axis integrator in the grid current loop is smaller than zero, and the output of the integrator declines. Whether the output of the integrator reaches the limiting value of the limiter depends on the amount of Pg. and Qg in the GC state. If the respective exchanging power Pg and Qgare large, then the reduction in igd is large when the grid is disconnected, and the output of the integrator will continue increasing until reaching the upper limiting value Vdmax. At that point, vdi will be fixed at Vdmax and vqi will be fixed at Vqmin. Then, the voltage references will change to the following equation:

$$\begin{cases} v_{Cdref} = k_{gp}.(i_{gdref} - i_{gd}) + V_{dmax} \\ v_{Cqref} = k_{gp}.(i_{gqref} - i_{gq}) + V_{qmin} \end{cases}$$

(20)

Conversely, if the respective amount of Pg and Qg are small, then the reduction of igd is small when the grid is disconnected, igd is regulated to equal igdref before the output of the integrator reaches Vdmax. Regardless of the case, the output of the integrator is always between the lower and upper limiting values of the limiter. The output of the integrator on the q-axis can be analysed similarly, and it consistently remains between Vqmin and Vqmax. By designing appropriate limiting values, during the transition from the GC state to SA state, the capacitor voltage amplitude can be controlled within the allowable operation range. 3) SA State: As indicated in Fig. 3, after islanding has been confirmed at time t2, Si turns OFF. There are several islanding detection methods, which can be classified into two groups, namely, remote and local. In this proposed control method, because the voltage amplitude and frequency are always controlled within the allowed range, the local passive methods are failed; the local active method, such as the method proposed in [35], can be used in the universal controller. The inverter operates in a VCM in the SA state; the P-regulator is adopted in the grid current loop, forming vcd–igd, vcq–igq droop control.To improve the voltage quality in the SA state, once islanding is detected at t2, vod switches from vdi to Vd0 and voq switches from vqi to Vq0, as shown in Fig. 2(b). Here, Vd0 is the nominal value of the capacitor voltage amplitude, and Vq0 is zero. The QR regulator GIG_QR in the grid current loop is also deactivated at t2, and the control formula of the grid current loop changes to (the following equation

$$\begin{cases} v_{Cdref} = V_{d0} + k_{gp}.(i_{gdref} - i_{gd}) \\ v_{cqref} = V_{q0} + k_{gp}.(i_{gqref} - i_{gq}) \end{cases} (21)$$

The real and reactive power can be shared approximately among DERs based on vc–ig droop control [36]–[38]. The output angular frequency ω* of FLL is determined by vcq, as shown in (10). The steady-state voltage error will be zero with the PI regulator GV _PI in the capacitor voltage loop; therefore, vcq serves as an intermediary between igq and ω*. The relationship between ω* and igqis presented in (22), and negative feedback results

$$\omega^* - \omega_0 = k_{FLL}.k_{gp}.(i_{gqref} - i_{gq}) \qquad (22)$$

If igq is not equally shared among DERs, according to (22), the angular frequency ω* of each inverter will differ, leading to a varying power angle δ. igq will also vary with varying power angle δ. Finally, ω* of each inverter converge to the same value, and equal sharing of igq can be achieved. The sharing of igd depends on grid line impedance. If the grid line impedances Zline of different DERs are the same, then igd can be shared equally. However, if Zline are different, then the vCd – igd droop relationship is useful for sharing igd. Even so, sharing error will persist due to unequal line impedance. For the capacitor voltage loop, the QR regulator GV _QR remains functional in the SA state to mitigate harmonics in the capacitor voltage. Because the QR regulator GIG_QR in the grid current loop is deactivated, the reference vh_Cdqref changes to zero. Harmonics in the capacitor voltage can be regulated to zero via the QR regulator GV _QR. 4) Transition From SA State to GC State: If the grid returns to normal and Su is closed, before turning ON Si, the PCC voltage vPCC should resynchronize with the grid voltage vg first. Three steps are adopted in the reconnection process to reduce the inrush grid current.

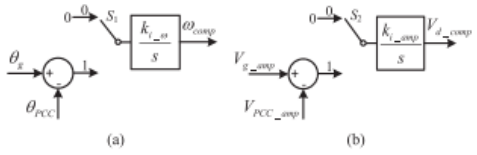


Fig. 5. Control block of (a) phase resynchronization and (b) voltage amplitude resynchronization.

First, when the grid returns to normal and switch Su turns ON, vod reconnects with vdi and voq reconnects with vqi, see Fig. 2(b). Second, the control switches S1 and S2 in Fig. 5 are connected with Channel 1 to realize amplitude and phase-angle resynchronization, where θg is the phase angle of the grid voltage, and θPCC is the phase angle of the PCC voltage; Vg_amp is the grid voltage amplitude, and VPCC˙amp is the PCC voltage amplitude; and ki_ω and ki_amp are the integral coefficients. Except for during the resynchronization process, the control switches S1 and S2 always connect with Channel 0. Third, Si turns to reconnect the MG with the utility. After some time, the limiter

output in the grid current loop becomes desaturated, and the PI regulator GIG_P I functions again. The QR regulator GIG_QR in the grid current loop is then activated, and the compensation terms ωcomp and V_d_compare reset to zero after the switch Si turns ON.

D. Discussion of the Effect of Load Change on Control Mode Switching

When the load brings a large step change in the GC state, the output of the integrator in the grid current loop can reach the limiting value of limiter, and the control method will switch from grid current control to vac –ig droop control. This occurrence may result in an undesirable transient process as explained. First, the influence of the local load change of one inverter on switching the control mode of parallel inverters is discussed. As displayed in Fig. 1, multiple inverters with the universal controller connect in parallel. When the local load of DER1 brings a large step change, the switching control mode of the inverters in DER1 and DER2 is analysed. The local active load of DER1 brings a large step change, increasing at instant t1. The d-axis capacitor voltagevCd1will then decline, as well the d-axis grid current igd1 at instant t1. As shown in Fig. 2(b), the input of the d-axis integrator in the grid current loop is larger than zero, and the output of the integrator increases. If the local load increase is large enough, the decline in igd1 is large and the output of the integrator will continue increasing to the upper limiting valueV_dmax. Then, the capacitor voltage reference will change to (23). The reduction in igd1 will cause an increase inv_(Cdref.)

$$v_{Cdref1} = k_{gp}.\left(i_{gdref1} - i_{gd1}\right) + V_{dmax} \qquad (23)$$

Due to regulation of the PI regulator in the capacitor voltage loop, the d-axis low v_(dref1.) the relationship between the capacitor voltagev_Cd1+ 〖jv〗 _Cq1 and PCC voltage v_PCCd+ 〖jv〗 _PCCq can also be represented as follows:

$$v_{Cd1} + jv_{Cq1} = (R_{line1} + jX_{line1}).(i_{gd1} + ji_{gq1}) + v_{PCCd} + jv_{PCCq} \qquad (24)$$

$$v_{Cd1} = R_{line1}i_{gd1} - X_{line1} + v_{PCCd} \qquad (25)$$

$$v_{Cd1} = R_{line1}i_{gq1} + X_{line1}i_{gd1} + v_{PCCq} \qquad (26)$$

Similarly, because in the MG application low voltage, the R/X ratio of line impedance is large, (25) and (26) can be simplified as follows:

$$v_{Cd1} = R_{line1}i_{gq1} + v_{PCCd} \qquad (27)$$

$$v_{Cq1} = R_{line1}i_{gq1} + v_{PCCq} \qquad (28)$$

The increase in vCd1 will stop the decline in igd1 and then cause an increase in igd1 according to (27). Therefore, the input of the d-axis integrator will decline, and the output of the integrator will reduce and gradually desaturation. The control method will ultimately return to grid current control from VC –ig droop control automatically. If the local reactive load of DER1 brings a large step increase, then the process is similar and is thus omitted here. The step change in the local load of DER1 has no influence on the control mode of the inverter in DER2; the power consumed by the local load of DER1 is provided by DER1, and the local load change is undertaken by DER1. The capacity of DER1 and its local load size should be designed carefully to ensure DER1 can provide the power consumed by the local load plus the power injected into the PCC. Second, the influence of the remote load change on switching the control mode of parallel inverters is analysed. If the grid is strong (i.e., the grid line impedance Zg in Fig. 1 is zero or small), when the remote load brings a large step change, it will be undertaken by the grid. Thus, it has no influence on the control mode of inverters in DER1 and DER2. While if the grid is weak (i.e., the grid line impedance Zg in Fig. 1 is large), the remote load change will influence the control mode of inverters in DER1 and DER2. When the remote load brings a large step increase at time t1, the output power of DERs remains nearly unchanged and is insufficient to meet remote load demand. Therefore, the amplitude and frequency of the remote load voltage falls and rises, respectively. Then, the analysis is similar with that during the transition from the GC state to SA state. It is easy to find that the d-axis grid current igd1 increases and igq1 declines at t1. As shown in Fig. 2(b), the input of the d-axis integrator in the grid current loop is smaller than zero, and the output of the integrator declines. If the increase of remote active load

is large, the increase of igd1 is large and the output of the integrator will continue decreasing until reaching the lower limiting value Vdmin. Then, the analysis is similar with the condition of local active load change, but the change direction of variables is reverse. The control method will ultimately return to the grid current control from the $_{vC}$ –ig droop control. Above all, no matter the local load of inverter or remote load brings a large step change in the GC state, if the control mode of inverter switches from the grid current control tov_C-i_g droop control, it can return to the grid current control automatically in the end, i.e., the control mode of inverters in DERs can achieve s*eamless sw*itchover.

III. Analysis and Design of Control Parameters

A. In this section, the inverter with a proposed universal controller is analysed and designed.

B. Analysis of Operating Points

In the GC state, the inverter is controlled as a current source by the grid current loop. The steady-state error of the fundamental component of the grid current is zero with the PI regulator in the grid current loop, and grid current harmonics are controlled to zero by QR regulators in the grid current loop and capacitor voltage loop; accordingly, the grid current in a steady state can be expressed by the following:

$$\begin{cases} i_{gd} = i_{gdref} \\ i_{gq} = i_{gqref} \end{cases} \quad (29)$$

In the SA state, the inverter is controlled as a voltage source, and the voltage reference is produced by vC –ig droop control. The steady-state error of the fundamental component of the capacitor voltage is zero with the PI regulator in a capacitor voltage loop, and capacitor voltage harmonics are controlled to zero by the QR regulator in the capacitor voltage loop; as such, the *capacitor voltage in a steady* state is as follows:

$$\begin{cases} v_{Cd} = V_{d0} + k_{gp}(i_{gderf} - i_{gd}) \\ v_{Cq} = V_{q0} + k_{gp}(i_{gperf} - i_{gq}) \end{cases} \quad (30)$$

C. *Limiter Design*

During the transition from the GC state to SA state, the outputs of the d- and q-axes limiters vdqi in the grid current loop can be different values according to the power flow direction of Pg and Qg in Fig. 1. According to the analysis in Section II-C, if the exchanging power Pg and Qg between the MG and utility in the GC state is small, then the output of the integrator may not reach the limiting values of limiter when the grid is disconnected. It is assumed that the exchanging power between the MG and utility is sufficient. When the MG disconnects from the utility, the output of the d-axis limiter vdi in the grid current loop is determined by Pg, as shown in (31); similarly, vqi is determined by Qg, as in (32), where vCd_GC and vCq_GC are output values of the d- and q-axes limiters at the moment when the MG is disconnected from the utility, respectively

$$v_{qi} = \begin{cases} V_{dmax}, & P_g > 0 \\ v_{Cd\_GC}, & P_g > 0 \\ V_{dmin}, & p_g > 0 \end{cases} \quad (31)$$

$$v_{qi} = \begin{cases} V_{dmin}, & P_g > 0 \\ v_{Cq\_GC}, & P_g > 0 \\ V_{dmin}, & P_g > 0 \end{cases} \quad (32)$$

If the MG injects real or reactive power into the utility in the GC state, then the DERs should reduce their output power when the MG disconnects from the utility, When the grid currents igd and igq of DER are each zero, the output power of DER reaches its minimum value (igdmin = 0 and igqmax = 0). Conversely, if the MG absorbs real or reactive power from the utility in the GC state, the DERs shall output more real or reactive power when the MG disconnects from the utility. The maximum value of the d-axis grid current igdmax and minimum value of the q-axis grid current igqmin are determined by the inverter power rating. Combing (20), (31), and (32), extreme values during the transition from the GC state to SA state can be calculated as listed in Table I.

According to the IEEE standard 1547-2018 [40], the allowed voltage operating range is 0.88–1.1Vnom, where Vnom is the nominal value of the capacitor voltage amplitude. Therefore, to ensure that the voltage magnitude is within the allowable range, the

chosen limiting values shall comply with the following rules:

$$\sqrt{(V_{dmax} - k_{gp}\,.\,(i_{gdmin} - i_{gdref}))^2 + (V_{qmin} - k_{gp}\,.\,(i_{gqmax} - i_{gqref}))^2} \leq 1.1\,.\,V_{nom} \quad (33)$$

$$\sqrt{(V_{dmax} - k_{gp}\,.\,(i_{gqmin} - i_{gdref}))^2 + V_{qmax} - k_{gp}\,.\,(i_{gqmax} - i_{gqref}))^2} \leq 1.1\,.V_{nom} (34)$$

$$\sqrt{(V_{dmin} - k_{gp}.\,(i_{gdmax} - i_{gdref}))^2 + (V_{qmin} - k_{gp}.\,(i_{gqmax} - i_{gqref}))^2} \geq 0.88.Vnom \quad (35)$$

$$\sqrt{(V_{dmin} - k_{gp}.\,(i_{gdmax-i_{gdref}}))^2 + (V_{qmin} - k_{gp}.\,(i_{gqmin} - i_{gqref}))^2} \geq 0.88.V_{nom} \quad (36)$$

The d-axis upper limiting valueV_dmax should exceed the nominal value V_nom,and the lower limiting valueV_dmin should be below the nominal valueV_nom, as shown in (37). In the GC state, vCq in a steady state is 0; thus,$V_{qmin}$and V_qmax should be symmetric, as indicated in (38)

$$\begin{cases} V_{dmax} > V_{nom} \\ V_{dmin} < V_{nom} \end{cases} \quad (37)$$

$$V_{dmin} = -V_{qmin} > 0 \quad (38)$$

The droop coefficient (proportional coefficient)K_gp is set to 0.4; the design procedure will be introduced later. The nominal phase-neutral capacitor voltage amplitude Vnom is 141.4 V. The d-axis grid current referencei_{gderf} is set to 5 A, andi_gqref is set to 0 A. The minimum of the d-axis grid current igdmin is zero, and the maximum igdmax is 10 A; the minimum of the q-axis grid current igqmin is –5 A, and the maximum igqmax is 0 A. Therefore, upon combining (33)–(38), we can select the limiting values as follows:

$$\begin{cases} V_{dmax} = 1.08\,.\,V_{nom} = 152.7\,V \\ V_{dmin} = 0.89\,.\,V_{nom} = 125.8\,V \\ V_{qmax} = 0.09\,.\,V_{nom} = 12.7\,V \\ V_{qmin} = -0.09.V_{nom} = -12.7V \end{cases} (3)$$

D. Controller Design

Design of Voltage Loop PI Regulator GV _PI: The voltage loop is used to regulate the capacitor voltage in GC and SA states, and the inner inductor current loop is used to improve the dynamic performance and damp the LC filter. For the inductor current loop, the small-signal model of the control-to-inductor current can be calculated as shown in (40). The transfer function of the delay introduced by digital control is represented by (41). The dual-updated operation mode of the program and pulse width modulation is adopted in digital control, such that the delay time Td in (41) is set to one switching cycle [15]

$$G_{id}(s) = \frac{i_L(s)}{d(s)} = \frac{V_{dc}}{2}.\frac{sCf}{s^{2Lf}C_f + sR_{ESR}C_f + 1} \quad (40)$$

$$H_d(s) = \frac{s^2\frac{T_d^2}{12} - s\frac{T_d}{2} + 1}{s^2\frac{T_d^2}{12} + s\frac{T_d}{2} + 1} \quad (41)$$

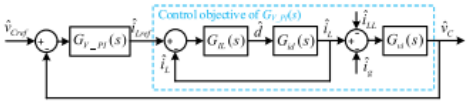


Fig. 6. Block diagram of the capacitor voltage loop and inductor current loop.

To simplify the design of inductor current loop, the delay is not considered in the derivation but will be covered in the final Bode plot. The P-regulator is adopted for GIL, as shown in (42). The transfer function from the capacitor current to capacitor voltage is presented in (43). Then, the control object of the voltage compensator (i.e., the transfer function from the inductor current reference to the capacitor voltage, see Fig. 6) can be gained, which is expressed in (44)

$$G_{IL} = k_{GII} \quad (42)$$

$$G_{vi}(s) = \frac{v_C}{i_C} = \frac{1}{sC_f} \quad (43)$$

$$G_{vi}(s) = \frac{V_{dc}}{2}.\frac{k_{GII}}{s^2 L_{fC_f} + s\left(R_{ESR}C_f + \frac{V_{ds}}{2}C_f k_{GII}\right) + 1} (44)$$

It is clear that (44) is a typical second-order system, and the damping factor ζ is related tok_GII. k_GII Can be calculated as (45). Therefore, k_GII can be designed according to the optimized damping factor ζ and is set at 0.0707

$$K_{GII} = \frac{2\xi\sqrt{\frac{L_f}{C_f} - R_{ESR}}}{\frac{V_{dc}}{2}} \approx \frac{4\xi}{V_{dc}}.\sqrt{\frac{L_F}{C_f}} (45)$$

Power stage parameters are shown in Table II, and the Bode plot of the control object of the voltage compensator is illustrated in Fig. 7 considering the delay

(41). Next, the voltage compensator GV _PI can be designed conveniently. A PI regulator, expressed by (46), is used for the voltage compensator GV _PI.

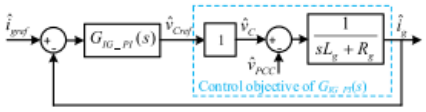


Fig. 7. Block diagram of the grid current loop.

$$G_{V_{PI}}(s)=k_{pv}+\frac{k_{IV}}{s} \quad (46)$$

2) Design of Grid Current Loop PI Regulator GIG_P I: Because the bandwidth of the capacitor voltage loop is much larger than that of the external grid current loop, the grid current loop can be designed based on the ideal voltage loop, in which the gain of the closed-loop transfer function is in unity within full frequency range. The control object of the grid current compensator can be simplified as (4), as illustrated in Fig. 9. The compensator GIG_P I of the grid current loop adopts different forms in the GC state and SA state, respectively. In theGC state, GIG_P I operates as a PI regulator, wherek_gp equals 0.4 andk_gi equals 180;

In the SA state, the compensator GIG_P I changes to a Pregulator, as shown in (21). To ensure that the load voltage magnitude is within the allowable range, the following rule should be obeyed:

$$\begin{cases} 0.88.V_{nom} \le v_{Cd}+k_{gp}.(i_{gdref}-i_{gd}) & \le 1.095.V_{nom} \\ -0.1.V_{nom} \le v_{Cq}=V_{q0}=k_{gp}.(i_{gqref}-i_{gq}) & \le 0.1.V_{nom} \end{cases} \quad (47)$$

Therefore, according to the setting values ofV_d, q0,i_gdqref the extreme values,i_gdqref and (47), the proportional coefficient kgp should comply with the following equation:

$$k_{gp} \le 2.68 \quad (48)$$

Ifkgp is selected to be larger, according to (33)–(36), to ensure the voltage amplitude remains within the allowable range during the transition from the GC state to SA state, the limiting values of the limiter on the d- and q-axes should be set closer to the nominal values. However, to maintain normal functioning of the integrator in the GC state, the limiting range of the limiter cannot be too narrow. There is a tradeoff when selecting the proportional coefficient kgp, which is ultimately set to 0.4 in this case.

The relationship between the angular frequency ω* and q-axis grid current igq is shown in (22). To ensure the angular frequency is within the allowable range [39], the following rule should be obeyed:

$$2\pi.49.8 \le \omega^* = \omega_0 + k_{FLL}.k_{gp}.(i_{gqref}-i_{gp}) \le 2\pi.50.2 \quad (49)$$

$$k_{FLL}.k_{gp} \le 0.08.\pi \approx 0.25 \quad (50)$$

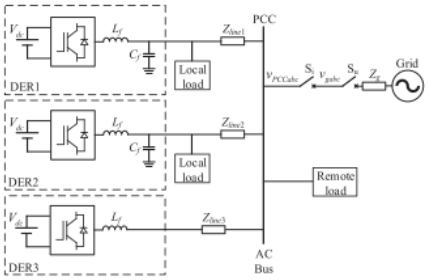


Fig. 8. Simulation circuit.

According to (50), when kgp is 0.4, the maximum of k_{FLL} is 0.625. In this article, k_{FLL} is set as 0.6. 3) Design of QR Regulator GIG_QR and GV _QR: In the grid current loop and capacitor voltage loop, the QR regulator is used to mitigate grid current harmonics in the GC state and capacitor voltage harmonics in *the SA state; see the following* equation:

$$G_{IG(V)_{QR}}(s)=\frac{2k_{ir6}\omega_c s}{s^2+2\omega_c s+(6\omega)^2} \quad (51)$$

In the GC state, the QR regulator GIG_QR is used to regulate the ±6th harmonics in grid current to zero, and GV _QR is used to regulate the ±6th harmonics in capacitor voltage to follow its reference vh_Cd,qref when the grid voltage including harmonics. In the SA state, GIG_QR in grid current loop is deactivated, the reference vh_Cdqref changes to zero. The harmonics in capacitor voltage can be regulated to zero by *the QR regulator* GV _QR.

The detailed design and analysis of the QR regulator have been discussed in [32].

With an increasing integral coefficient kir6, the gain of QR regulator at the resonance angular frequency increases. With a growing cut-off frequency ωc, the gain and
bandwidth of the QR regulator increase. Yet, an excessively large kir6 will deteriorate the stability and convergence of the system, and an overly large ωc will influence the frequencyselection characteristic of the regulator. Thus, there is a tradeoff when selecting the integral coefficient kir6 and cut-off frequency ωc. In this article, kir6 is set to 30 and ωc is set to 5 rad/s.

IV.FUZZY LOGIC CONTROLLER

In this paper presents a Fuzzy Logic Controller as an extension method to improve system performance, The Structure of the system is shown below

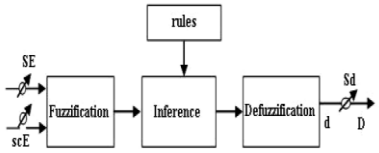


Fig.9 General Diagram of a fuzzy controller

The info E (k) appears if the heap task point at the moment k is situated on the left or on the privilege of the greatest power point on the PV trademark, while the information CE (k) communicates the moving heading of this point. The fuzzy surmising is done by utilizing Madman's strategy,, and the defuzzification utilizes the focal point of gravity to figure the yield of this FLC which is the obligation cycle

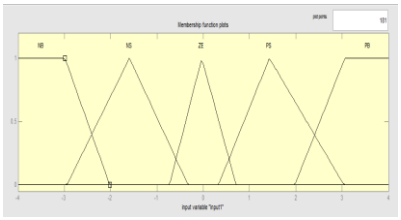


Fig.10 Input-1 Error membership function

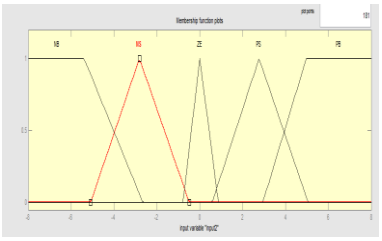


Fig.11 Input-2 Change in Error membership function

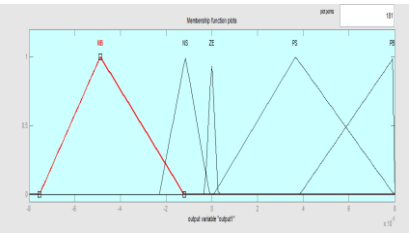


Fig. 12 *output membership function*

Table – 1: *Fuzzy Logic Controller Rules*

E/ΔE	NB	NS	ZE	PS	PB
NB	ZE	PS	PS	ZE	NS
NS	PB	PS	ZE	ZE	NS
ZE	PB	PS	ZE	NS	NB
PS	PS	ZE	NS	NB	NB
PB	PS	ZE	NS	NS	ZE

SIMULATION RESULTS:

Case1

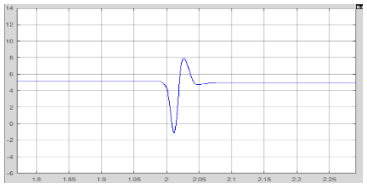


Fig13 d-axis grid current igd1 of master DER1

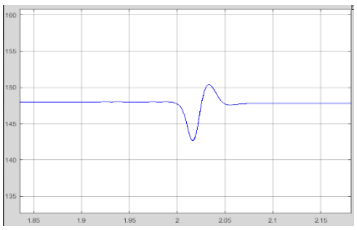


Fig 14 d-axis capacitor voltage vCd1 of master DER1

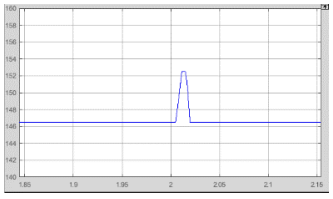


Fig 15 Output of the d-axis limiter in grid current loop of master DER1

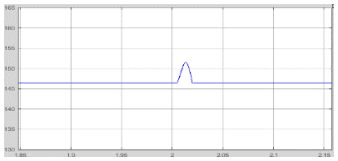


Fig 16 d-axis capacitor voltage reference vCdref1 of master DER1

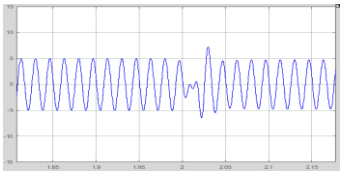


Fig 17 Phase a grid current iga1 of master DER1

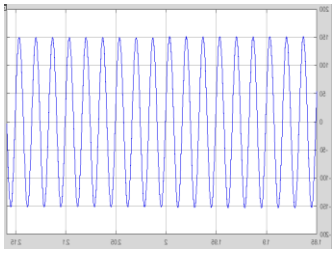


Fig 18 Phase A capacitor voltage vCa1 of master DER1

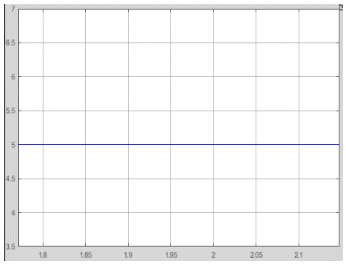


Fig 19 d-axis grid current igd2 of master DER2

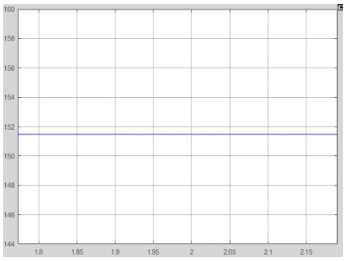


Fig 20 d-axis capacitor voltage vCd2 of master DER2

Case2

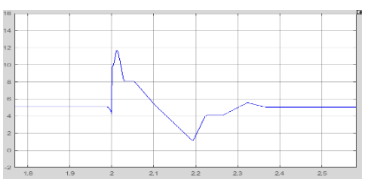


Fig 21 d-axis grid currentigd1

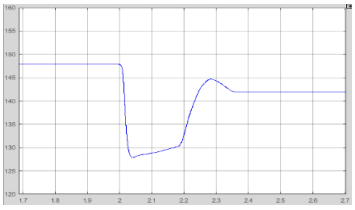


Fig 22 d-axis capacitor voltage vCd1

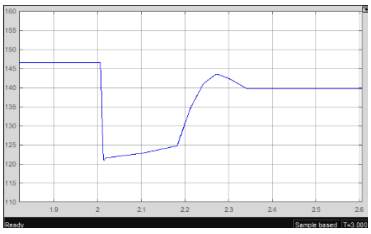


Fig 23 Output of the d-axis limiter in grid current loop

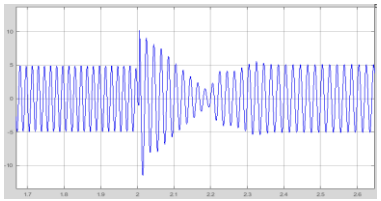


Fig 24 d-axis capacitor voltage reference vCdref1

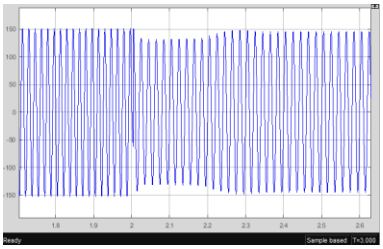


Fig 25 Phase A grid current iga1

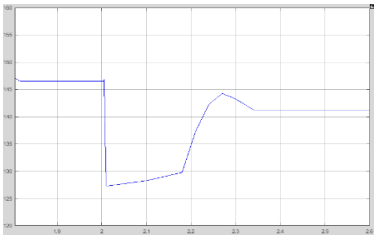


Fig 26 Phase A capacitor voltage vCa1

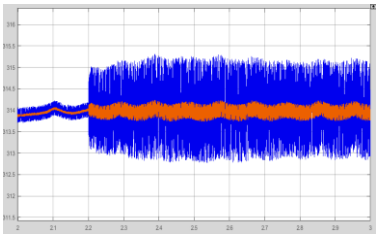


Fig 27 Simulation waveforms of angular frequency produced by original FLL (blue line) and SOGI-QSG-based FLL (red line)

VI. CONCLUSION

A universal controller for parallel inverters with fuzzy logic controller is suggested for multiple operating states, which can achieve distinct goals in the Grid linked and Standalone stages and provide seamless transition between these states. The necessity to switch between two sets of controllers can be avoided by designing such a controller. The suggested controller can achieve precise grid current regulation of the inverter in the GC mode. When islanding occurs, the proposed controller can switch from grid current control to VC –ig-based droop control automatically, eliminating the need for islanding detection.